AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 23 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit;

one or more first registers configured to couple one or more input signals to said non-programmable hard wired blocks; and

one or more second registers configured to receive one or more output signals from said non-programmable hard wired blocks.

2. (ORIGINAL) The apparatus according to claim 1, wherein said one or more logic circuits comprise variable width logic circuits.

3. (ORIGINAL) The apparatus according to claim 2, wherein a width of each of said one or more logic circuits is determined in response to one or more input signals.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to receive one or more inputs comprising one or more of a multi-bit signal and a single-bit signal in one or more of a serial configuration and a parallel configuration.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein one or more of said non-programmable hard wired blocks comprises a hard wired multiplier.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein one or more of said non-programmable hard wired blocks are configured to perform cyclic redundancy check (CRC) functions.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein one or more of said logic circuits are configured to present one or more outputs.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said one or more outputs comprise intermediate signals.

9. (ORIGINAL) The apparatus according to claim 7, further comprising:

an adder circuit configured to receive said one or more outputs.

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said routable interconnect circuit is configured to route one or more of signals to one or more of said non-programmable hard wired blocks and signals from one or more of said non-programmable hard wired blocks.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 10, further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

12. (ORIGINAL) The apparatus according to claim 1, wherein each of said one or more logic circuits comprise an input portion configured to store one or more input signals.

13. (ORIGINAL) The apparatus according to claim 12, wherein each of said one or more logic circuits comprises an output portion configured to store an output.

14. (CANCELED)

15. (CURRENTLY AMENDED) An apparatus comprising:

means for receiving one or more input signals; ~~and~~

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit;

means for storing one or more input signals to said non-programmable hard wired blocks; and

means for storing one or more output signals from said non-programmable hard wired blocks.

16. (CURRENTLY AMENDED) A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within said programmable logic device, wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit;

(C) storing one or more input signals to said non-programmable hard wired blocks; and

(D) storing one or more output signals from said non-programmable hard wired blocks.

17. (CURRENTLY AMENDED) The method according to claim 16, further comprising the step of:

(~~C~~E) generating one or more ~~output signals~~ outputs.

18. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein step (B) further comprises:

multiplying said one or more input signals with one or more of said hard wired blocks.

19. (PREVIOUSLY PRESENTED) The method according to claim 17, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. (CURRENTLY AMENDED) The method according to claim 17, wherein step (~~e~~E) further comprises:

routing said one or more outputs with said routable interconnect circuit.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said non-programmable hard wired blocks comprise dedicated logic having a fixed implementation of a given functional block on silicon.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said programmable elements comprise configurable macrocells.

23. (CANCELED)

24. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said non-programmable hard wired blocks (i) comprise hard wired multipliers having a first width and (ii) are couplable to form one or more multipliers having a second width.

25. (NEW) An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions, (ii) connectable by a routable interconnect circuit and (iii) each of said one or more logic circuits is configured to receive one or more inputs comprising one or more of a multi-bit signal and a single-bit signal in one or more of a serial configuration and a parallel configuration.